

IN THE CLAIMS

No amendments are made by the present response. The text of all pending claims, along with the corresponding status indicators, is set forth below:

1. (previously presented) A system comprising:
 - a processor;
 - a main memory operably coupled to the processor;
 - a cache memory operably coupled to the processor; and
 - a host controller coupled between the processor and the main memory and configured to coordinate the exchange of a request and data associated with the request between the processor, the main memory and the cache memory, the host controller comprising:
 - a memory controller operably coupled to the main memory;
 - a processor controller operably coupled to the processor;
 - a coherency controller operably coupled to the cache memory; and
 - an internal bus structure configured to couple each of the memory controller, the processor controller and the coherency controller to each other, the internal bus structure comprising a plurality of individual buses, wherein the internal bus structure is configured to transmit the request comprising a plurality of ordered transactions each having a unique signal type, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request.

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2. (original) The system, as set forth in claim 1, wherein each of the plurality of individual buses is coupled only between two of the memory controller, the processor controller and the coherency controller.

3. (original) The system, as set forth in claim 2, wherein the plurality of individual buses is coupled between the memory controller and the processor controller.

4. (original) The system, as set forth in claim 2, wherein the plurality of individual buses is coupled between the memory controller and the coherency controller.

5. (original) The system, as set forth in claim 2, wherein the plurality of individual buses is coupled between the processor controller and the coherency controller.

6. (previously presented) The system, as set forth in claim 1, wherein each signal type corresponds to a single transaction in the particular request operation.

7. (original) The system, as set forth in claim 6, wherein each respective signal type includes an identification tag.

8. (original) The system, as set forth in claim 7, wherein the identification tag comprises a source identification, a destination identification, and a cycle identification.

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9. (original) The system, a set forth in claim 8, wherein the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete.

10. (original) The system, as set forth in claim 1, wherein the processor comprises the cache memory.

11. (original) The system, as set forth in claim 1, comprising:
a plurality of processor buses;
a plurality of processing units, wherein each processing unit is coupled to a respective one of the plurality of processor buses; and
a plurality of processor controllers, each processor controller corresponding to a respective one of the plurality of processor buses, wherein the processor controllers are not directly coupled to each other via the internal bus structure.

12. (previously presented) An internal bus structure of a host controller comprising a plurality of individual buses, wherein the internal bus structure is configured to transmit a request comprising a plurality of ordered transactions each having a unique signal type, and each of the individual buses comprising a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of data associated with the request.

13. (original) The internal bus structure, as set forth in claim 12, wherein each individual bus is coupled between only a first controller and a second controller.

14. (original) The internal bus structure, as set forth in claim 13, wherein the first controller comprises a processor controller .

15. (original) The internal bus structure, as set forth in claim 13, wherein the second controller comprises one of a memory controller and a coherency controller .

16. (previously presented) The internal bus structure, as set forth in claim 12, wherein each signal type corresponds to a single transaction in the particular request operation.

17. (original) The internal bus structure, as set forth in claim 16, wherein each signal type includes an identification tag.

18. (original) The internal bus structure, as set forth in claim 17, wherein the identification tag comprises a source identification, a destination identification and a cycle identification.

19. (original) The internal bus structure, as set forth in claim 18, wherein the cycle identification includes a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete.